THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
SILVER SPRING, MARYLAND

S1P-581-70
August 14, 1970

TO: R. E. Cashion

FROM: C. Cunningham

SUBJECT: Modification of Rate Limiters and Interface Circuits for CPME.

The modifications to the rate limiters and interface circuits described herein are intended to correct a trigger problem in the rate limiters which has risen in testing the assembled CPME. Furthermore, they are intended to insure that some previously overlooked rise and fall time constraints on the output pulses are met. Specifically, the Project Office has requested that rise and fall times between +0.5v and +5.0 volts be greater than 0.2 μsec.

The trigger problem in the rate limiters has been found to be due to capacitive loading on the output of the rate limiters, which seems to result primarily from the stray capacitance encountered in the wiring harnesses to the flight and test connectors.

This capacitance was underestimated in the initial design of the rate limiters. In addition, the rate limiters will be required to drive an additional 30 - 40 pf of capacitance which appears across the accumulator inputs in the spacecraft.

The present rate limiter circuit is shown in Figure 1. The modified circuit is shown in Figure 2. The proposed modifications are as follows:

1. Add resistors in series with rate limiter outputs, as shown in Figure 2. These partially decouple the load capacitance from the timing loop allowing a faster rise-time pulse at the timing point which serves to insure that the pulse will rise to the gate threshold voltage within the width of the trigger pulse. Furthermore, the series resistors, in conjunction with the load capacitance, serve to limit the rates of rise and fall of the output pulse as seen at the spacecraft interface. The series resistors will also serve to limit the current which can be drawn from the circuits in the event that one of the outputs is short-circuited. The series resistors are to be 3 KΩ for those outputs which drive rate registers (Z_{in} = 24K), and 2 KΩ for those outputs which drive sectored registers (Z_{in} = 10K). These resistors will also be included in series with the outputs from the sectored data commutator and the in-flight calibrator sub-commutator.

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2. Increase logic supply voltage from +8V to +9V. This increases the available gain of the MOSFETS, within the COS/MOS gates, particularly the P-channel pull-up devices. This improves rise and fall times and reduces propagation delays, thereby, decreasing the "minimum width-to-trigger". The series resistors have been chosen to insure that the maximum permissible signal level is provided to the spacecraft accumulators.

3. Increase output pulse width from 1.0 μsec to 1.8 μsec by increasing the timing capacitor. This has been found to improve triggering considerably, in that the longer timing time-constant serves to insure that the pulse amplitude at the "hold-on" gate has reached the threshold level within the width of the trigger. The "dead-time" between pulses will remain at approximately 1 μsec. This will lower the limiting rate to approximately 3×10^5 c/s; however, the only channels that might ever exceed this rate are the scintillator channels M and S. On these channels, the pulse width may remain at 1.0 μsec to accommodate the higher counting rates since the rate limiters on these two channels are triggered by pulses whose width is approximately 0.6 μsec and therefore, there has been no difficulty encountered on these channels.

4. Increase strobe widths by approximately 50 nanoseconds. This is not absolutely essential, but is very desirable to provide some additional margin in trigger width.

A rate limiter board has been constructed and tested with these modifications incorporated. The primary timing capacitors were increased to 47 pf to provide an output pulse width of approximately 1.8 μs (FWHM). These were tested for various conditions of supply voltage, trigger amplitude and width, and load capacitance. Some of the test results are tabulated in Figure 3. The meanings of the various terms are explained following the table and are further illustrated in Figure 4.

A more complete description of the rate limiter circuits will be included in the documentation on the logic and interface sections of the experiment. Completion of this documentation is presently being delayed until the latest revisions of the channel logic are completed. The modifications described herein are presented so that they may be incorporated into the rate limiter and sub-commutator PC boards. It appears that they will completely resolve the trigger problem and provide more than adequate design margins. A list will be prepared to indicate which resistors will be 3K and which will be 2K.

C. Cunningham
C. Cunningham

CC:ks
Distribution page 3

Distribution:
COBostrom
SMKrimigis
RECashion
SAGary
DPPeletier
JWKohl
JTMueller
AFHogrefe
Archives (2)
File

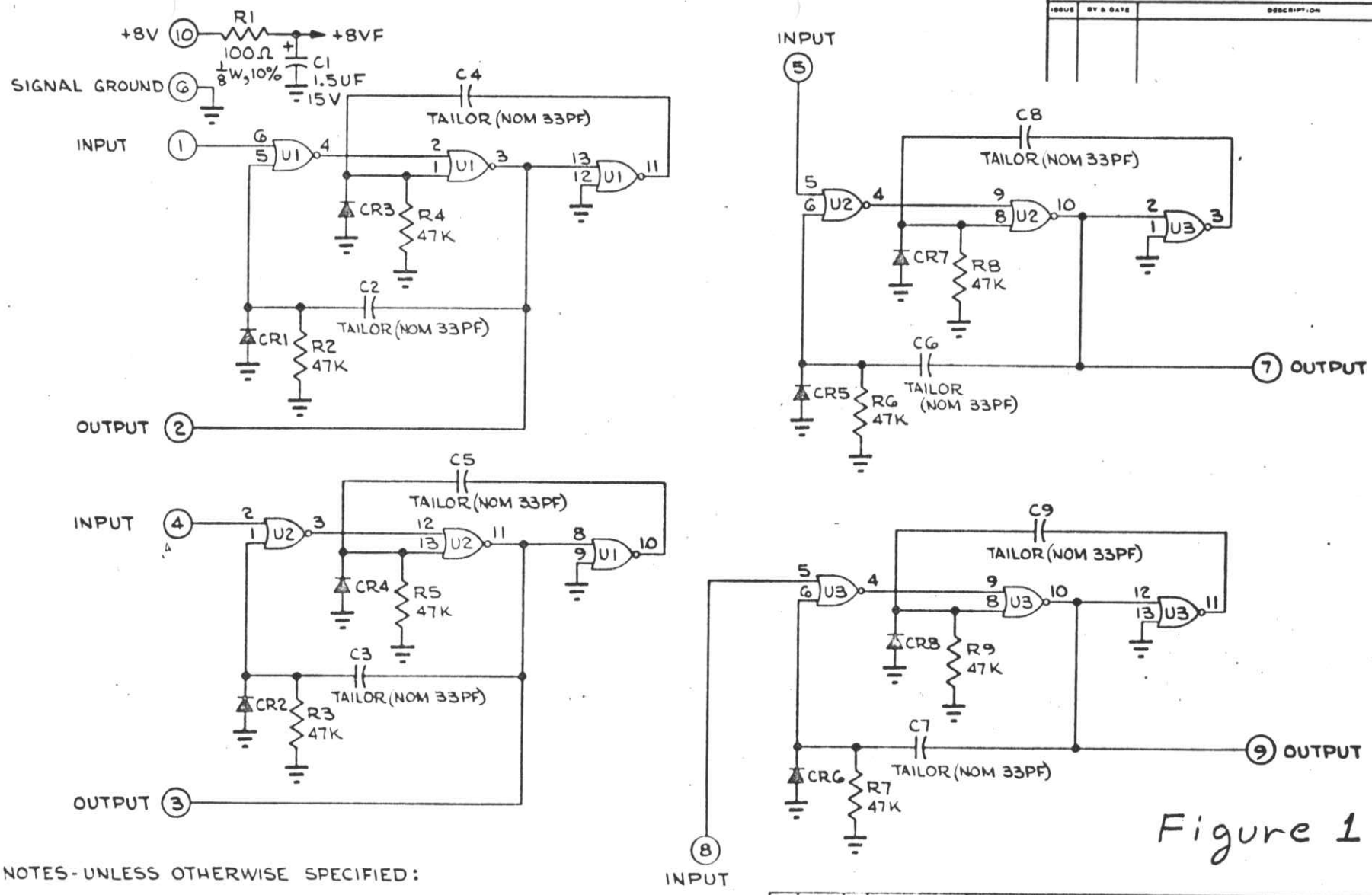

Figure 1

NOTES - UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/8W, 5%
2. ALL DIODES ARE TXIN3064
3. ALL INTEGRATED CIRCUITS ARE CD4001 RCA
4. PIN 7 OF I.C.'S ARE GRD; PIN 14 OF I.C.'S ARE +8VF

HIGHEST REF DESIGNATION	
R9	C9
CR8	U3

REVISIONS

ISSUE	BY & DATE	DESCRIPTION	CHECK	APPROVED & DATE

LIST OF MATERIAL

BASE QTY ASSY	ITEM NO	DWG SIZE	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR CODE	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	MFG CODE	ISSUE REV.
		A	SRA-G528	REF					
		C	SRA-G527	REF					
SRA-G525		C	SRA-G526	REF					

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
XX = ± .03
XXX = ± .010
ANGULAR = ± 2°
DIM & TOL PER MIL STD 86
BREAK SHARP EDGES REMOVE ALL BURRS

J.T. MUELLER 2 MAR 70

THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
8621 GEORGIA AVENUE SILVER SPRING MARYLAND

SCHEMATIC DIAGRAM
OUTPUT RATE LIMITER & PULSE SHAPER
CPME
IMP H+J SATELLITE

CODE IDENT NO	SIZE		ISSUE
88898	C	SRA-G525	a

SCALE — SHEET 1 OF 1

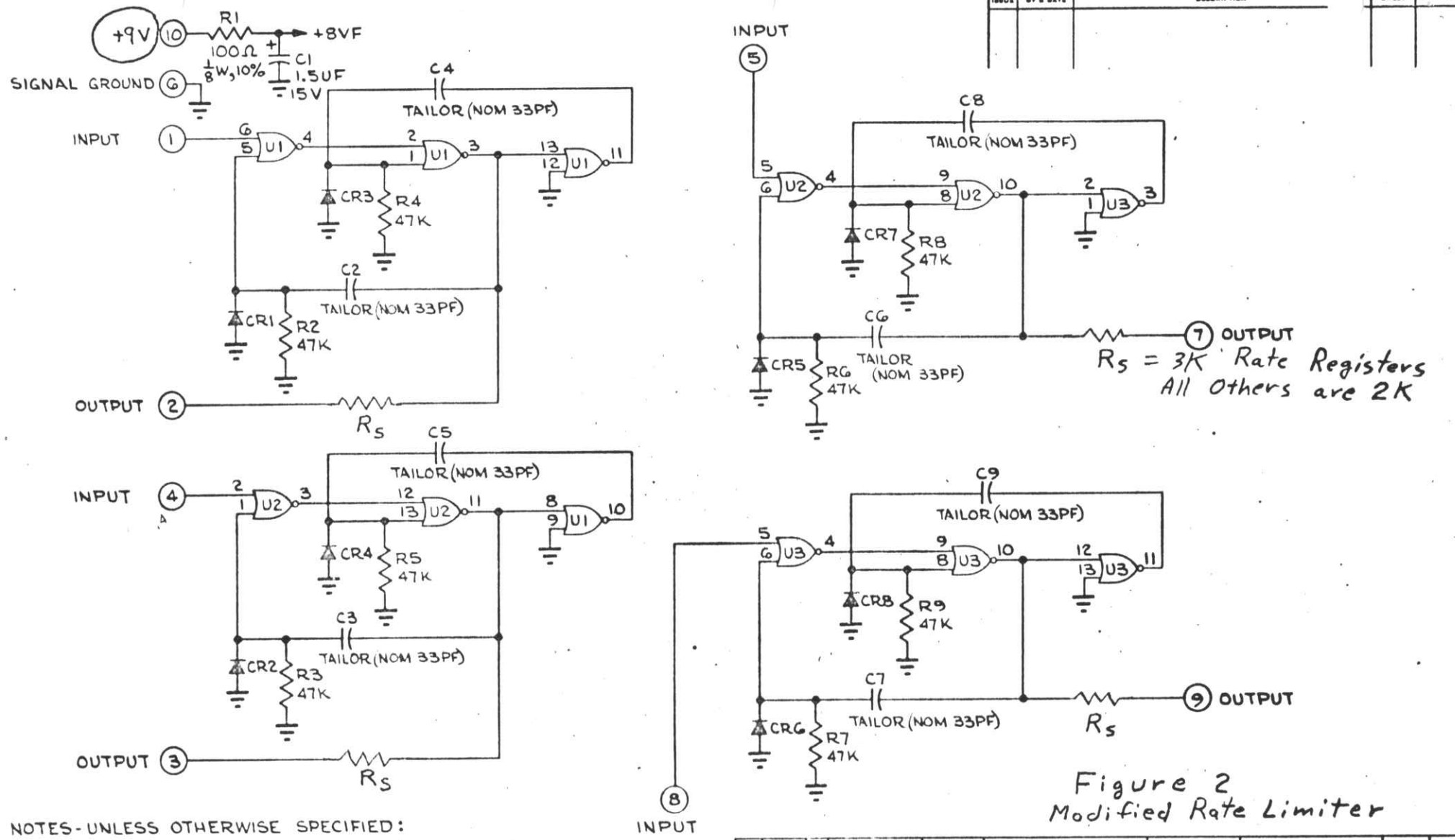

Figure 2
Modified Rate Limiter

NOTES - UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/8W, 5%
2. ALL DIODES ARE TXIN3064
3. ALL INTEGRATED CIRCUITS ARE CD4001 RCA
4. PIN 7 OF I.C.'S ARE GRD; PIN 14 OF I.C.'S ARE +9VF

HIGHEST REF DESIGNATION	
R9	C9
CR8	U3

REVISIONS

ISSUE	BY & DATE	DESCRIPTION	CHECK	APPROVED & DATE

LIST OF MATERIAL

BASIC ASSY	ITEM NO	DWG SIZE	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR IDNO	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	MFR CODE	ISSUE REV
			SRA-G525						
			SRA-G528	REF					
			SRA-G527	REF					
			SRA-G526	REF					

PART NUMBER | SIZE | NEXT ASSEMBLY | QTY PER | USED ON | EFFECTIVITY (SHIP/TER SER NO) | WEIGHT

SURFACE TREATMENT (BEFORE ASSY) | SURFACE ROUGHNESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
XX = ± .03
XXX = ± .010
ANGULAR = ± 2°
DIM & TOL PER MIL STD 68
BREAK SHARP EDGES REMOVE ALL BURRS

J.T. MUELLER 2 MAR 70
DRAWN BY | PROJ | DATE
HECK | DATE | STRESS | DATE
GROUP | DATE | THERMAL | DATE
SYSTEM | DATE | RF | DATE
RELIABILITY | QUAL | ATTITUDE | DATE
RELEASE (INITIAL) | | POWER | DATE

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SCHEMATIC DIAGRAM
OUTPUT RATE LIMITER & PULSE SHAPER
C P M E
IMP H + J SATELLITE

CODE IDENT NO	SIZE		ISSUE
88898	C	SRA-G525	a

SCALE | DO NOT SCALE PRINT | SHEET 1 OF 1

	R_L	C_L	R_S	V_{DD}	SA	SW	τ_r	τ_f	V_o	FWHM
1)	24K	100 pf	3K	9V	8V (5V min)	200ns (70ns min)	0.4 μs	0.8 μs	7.8V	1.8 μs
2)	24K	75 pf	3K	9V	8V (5V min)	200ns (60ns min)	0.3 μs	0.6 μs	7.8V	1.8 μs
3)	10K	100 pf	2K	9V	8V (5V min)	200ns (70ns min)	0.35 μs	0.5 μs	7V	1.75 μs
4)	10K	75 pf	2K	9V	8V (5V min)	200ns (70ns min)	0.28 μs	0.28 μs	7V	1.75 μs

Notes:

1) Cases 1 and 2: Limiting Rate $\approx 3.4 \times 10^5$ c/s (Periodic Input)
2) Cases 3 and 4: Limiting Rate $\approx 3.5 \times 10^5$ c/s (Periodic Input)
3) Cases 1 and 2: V_{DD} (min) ≈ 6.6V
   Cases 3 and 4: V_{DD} (min) ≈ 6.8V
4) In addition, the rate limiters were tested with R_L = 10K, C_L = 200 pf and V_{DD} = 9V. Completely reliable triggering was obtained with trigger widths as small as 120 ns and the output pulse rise and fall times (0.5v - 5v) were 0.8 μs and 120 ns, respectively.

Figure 3

Test Results-Modified Rate Limiter

The terms used are defined as follows:

R_L = Load Resistance
C_L = Load Capacitance
R_S = Series Resistor in Rate Limiter Circuit
V_{DD} = Drain Supply Voltage
SA = Strobe Amplitude
SW = Strobe Width
τ_r = Output Pulse Rise-Time (0.5v - 5v)
τ_f = Output Pulse Fall-Time (5v - 0.5v)
V_o = Output Pulse Height (Volts)
FWHM = Width of output pulse at half-maximum.

These are shown in Figure 4.

Figure 4

Modified Rate Limiter Circuit
Showing Input and Output Conditions